UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,642	07/07/2003	Charutosh Dixit	03-0169 (4028-03200)	7652

24319 7590 02/24/2006

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,642	DIXIT ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 07 July 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-30 are presented for examination.

Drawings

The drawings are objected to because descriptive labels other than numerical are needed for figure 2. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 4, 15, 16, 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "about zero" in claims 3, 15 and 25 is a relative term, which renders the claim indefinite. The term "about zero" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. In a general sense “about zero” relative to eternity could be 1 year, or relative to an hour could be one minute. These claims will not be further considered on their individual merits.

The term "about 500 ms" in claim 16 is a relative term which renders the claim indefinite. The term " about 500 ms " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. This claim will also not be further considered on its merits.

Claim 4 is dependent on claim 3 and therefore inherits the 35 U.S.C. 112, second paragraph issues of the claim 3 and may also not be further considered on the merits.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 5-14, 16-24, and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwarz U.S. Patent No. 5,835,429 in view of Schwarz et al. U.S. Patent No. 6,496,947.

As per claims 1, 9, and 22, Schwartz substantially teaches the claimed method of testing for data retention faults in which the memory array power supply voltage is dropped allowing the memory array to advance to a standby mode. While the memory array is in the standby mode, the amount of current that is able to flow into a memory cell is sufficiently decreased that defective cells are not able to replenish the charge lost due to leakage. In short, the cell will no longer be able to hold data. After a sufficient pause to allow the leakage to take effect in the defective cells, the memory power supply voltage is restored to its nominal value and the memory array output is read for the purpose of determining whether any cell data has been flipped from its previous setting. (Column 1 lines 45-54) Not disclosed by Schwartz is that data is written into segments and then paused and then read.

However, in an analogous art, Schwartz et al teach the integrated circuit has a built-in self repair (BISR) circuit which executes a sequence of read and write

operations on a memory array and a pause circuit which pauses the sequence of write and read operation for a pause time period. (Column 2 lines 17-27) Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the method of pausing disclosed by Schwartz et al., with the testing method of Schwartz. This would have been obvious as suggested by Schwartz (column 1 lines 50-54) since the data retention is caused by leakage the pause would be necessary to see if the cell leaks.

As per claims 2, 6-8, 17-20, and 26-29 Schwartz teaches, writing a pattern of data to the memory array utilizing a normal write cycle. The pattern is then read back from the memory array and compared for accuracy. Next, an inverse pattern is written to the memory array. The original pattern is again read from the memory array allowing the detection of any cell with flipped data. This process is then repeated using inverted data for the initial write cycle, followed by a write cycle with inverse data. In this manner, the algorithm can verify that all cells in the memory array can hold two state binary information. For an even more thorough and meticulous testing procedure, the write patterns can be varied for example from zeros, to ones, to checker boards. (Column 2 line 55 through column 3 line 5)

As per claim 5, this is merely a repetition of the steps from step 1 and repeating the write and read and pause steps would only provide a more thorough test procedure, (Schwartz et al Column 2 lines 17-26)

As per claim 10 – 14, Schwartz et al. teaches the claimed controllers (column 3 lines 1-47 Figure 7) with the exception of the JTAG controller, however it would have

been obvious to a person having ordinary skill in the art at the time this invention was made to have used JTAG controllers with the interface described by Schwartz et al. as the IEEE 1149.1 is the industry standard in the claimed area.

As per claims 21, and 30, Schwartz et al teach the memory sub groups are on a single chip (column 9 lines 1-10).

As per claims 23 and 24, Schwartz et al teach accessing means for each group of memory arrays. (column 2 lines 12-27).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"An Efficient BIST Method for Testing of Embedded SRAMs" by Tehranipour et al. International Symposium on Circuits and Systems, 2001 Publication Date: 2001 Volume 5, pages 73-76 ISBN: 0-7803-6685-9INSPEC Accession Number: 7042567

This paper teaches developing an algorithm to enable conventional microprocessors to test their on-chip SRAM using their existing hardware and software resources. This test method utilizes a mixture of existing memory testing techniques, which cover all important memory faults. This is achieved by writing a routine called BIST Program, which only uses the existing ROM and creates no additional hardware overhead. BIST Program implements the "length 9N" test algorithm. The proposed test

algorithm covers 100% of faults under the fault model plus a data retention test. A memory faults diagnostic capability is also provided by the BIST Program. This method can be implemented for embedded SRAM testing of all microprocessors, microcontrollers and DSPs. This test algorithm is experimented on 32 K SRAM of the Texas Instruments TMS320C548 DSP

"Quick Address Detection of Anomalous Memory Cells in a Flash Memory Test Structure" by Himeno,et al. IEEE Transactions on Semiconductor Manufacturing, Publication Date: May 1997 Volume: 10, Issue: 2 pages: 196-200 INSPEC Accession Number: 5570257

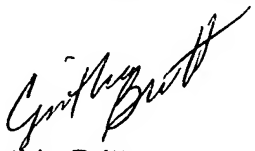
This paper teaches a scheme for quick address detection of anomalous memory cells having the highest and lowest threshold voltages in a flash memory test structure is described. A test structure with a large memory cell array has been developed to evaluate reliability of flash memory cells before fabrication of a new generation of flash memory devices. In this test structure, each terminal branch of a tree-structured column selector is connected to each bitline of the array. And a simple threshold voltage distribution monitor circuit (VTDM) which has been proposed is connected to the other end of the bitlines. A proposed Multi-Address Scanning Scheme (MASS) is performed by the tree-structured column selector with monitoring the output of VTDM. The detection time has been reduced to 1.12% in the case of 2048 columns. This is suitable

for performing reliability tests, such as program/erase endurance test and data retention test.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Cynthia Britt
Examiner
Art Unit 2138